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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,044	CALLAGHAN, DAVID M.	
	Examiner	Art Unit	
	Matt Urick	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/18/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-43* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 7-9, 11, 13-16, 18, 22, 23, 26, 27, and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Callaway (United States Patent No. 6,879,530).

As per claim 1, Callaway discloses:

A self-testing random access memory (RAM) system for a computer, comprising:

a memory array (figure 1 memory blocks 50-53); and

a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array, tests integrity of data stored in the memory array (column 4 lines 13-28 and figure 1: test and repair circuitry 58)

the self-testing RAM interface with the memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits (column 9 line 65 – column 10 line 8).

Test and repair circuitry 58 is responsible for (a) writing addresses to storage, (b) determining if faults are found, and (c) remapping memory blocks if faults are found. Callaway does not use the word "microprocessor" to describe this element, but because it is capable of interpreting instructions, performing logic operations, and controlling write and read functions of the system, it meets the definition of a processor.

As per claim 2, Callaway discloses:

The system of claim 1, the self-testing RAM interface interacts with a central processing unit (CPU) to test the CPU to memory interface (column 4 lines 15-18 and figure 6: the testing may interact with BIOS, which is stored on the processor device 36).

As per claim 4, Callaway discloses:

The system of claim 1, the self-testing RAM interface can correct errors in data stored in the memory array (column 10 lines 55-59).

As per claim 7, Callaway discloses:

The system of claim 6, the self-testing R.AM interface includes a memory component that facilitates execution of testing and/or correcting algorithms (column 4 lines 10-13).

As per claim 8, Callaway discloses:

The system of claim 1, the self-testing interface is implemented with discrete logic (column 4 lines 58-64).

As per claim 9, Callaway discloses:

The system of claim 1, the self-testing RAM interface is implemented using SOC (System on Chip) technology (figure 1: the system is exists on memory 40).

As per claim 11, Callaway discloses:

The system of claim 1, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices (column 10 lines 16-29)

As per claim 13, Callaway discloses:

The system of claim 1, the self-testing RAM interface supports multi-port memory Access (column 6 lines 1-13).

As per claim 14, Callaway discloses:

A self-testing and self-validating memory system comprising:

one or more memory storage banks (figure 1); and

at least one central processing unit (CPU) with a self-testing RAM interface subsystem for ensuring correct data retrieval (column 4 lines 13-28 and figure 1: test and repair circuitry 58)

a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards (column 9 line 65 – column 10 line 8).

As per claim 15, Callaway discloses:

The system of claim 14, the storage banks comprising standard RAM components with internal flaws (column 2 lines 51-55)

As per claim 16, Callaway discloses:

The system of claim 14, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices (column 10 lines 16-29).

As per claim 18, Callaway discloses:

The system of claim 14, the self-testing R.AM interface acts as a virtual memory manager and maps received data to multiple copies of the data in different memory banks to enable correct data retrieval (column 2 lines 57-62).

As per claim 22, Callaway discloses:

A method of self-testing comprising:

writing values to one or more memory cells in a memory device (figure 9 step 112),

reading the values stored by the one or more memory cells (figure 9 step 114);

comparing the values written with the values read (figure 9 step 116); and

notifying a central processing unit if any of the values written differ from the values read (column 11 lines 18-25, the system may interact with the BIOS or processor 36), wherein writing values, reading a value, comparing values, and notifying a central processing unit are performed by a self-testing RAM interface (column 4 lines 13-28), the self-testing RAM interface further comprising a microprocessor, the self-testing RAM interface is embedded with the memory cells on a single circuit board (column 4 lines 13-28).

As per claim 23, Callaway discloses:

The method of claim 22, the values written correspond to a test pattern (column 4 lines 48-50).

As per claim 26, Callaway discloses:

The method of claim 22, further comprising bringing the memory device on-line for use upon successful test completion (column 10 lines 55-59).

As per claim 27, Callaway discloses:

An article of manufacturing comprising a computer usable medium having computer readable stored instructions thereon to perform the method of claim 26 (column 4 lines 13-28: test and repair circuitry is an article of manufacture storing computer readable instructions).

As per claim 43, Callaway discloses:

The system of claim 1, wherein upon computer system start-up, the self-testing RAM interface effectuates all testing procedures to make portions of tested RAM available to the CPU while CPU concurrently runs boot process (column 11 lines 18-25: the BIOS, which is the boot process, may assist in testing and remapping).

Claim 20 is rejected under 35 U.S.C. 102(e) as being unpatentable over Ouellette (US Patent No. 6,993,692). Ouellette discloses:

A self-correcting and self-validating RAM device (column 2 lines 52-59) comprising:

a plurality of internal memory stores (column 2 lines 44-47, lines 52-59); and

a microprocessor embedded with the memory stores on a circuit board (column 2 line 60 – column 3 line 4);

a self-testing interface that includes the microprocessor and maps input addresses and data to a multitude of memory cells on a plurality of memory stores to

facilitate accurate data storage and retrieval, wherein the memory cells store copies of the input data (column 4 lines 25-34).

Claims 34, 35, and 42 are rejected under 35 U.S.C. 102(e) as being unpatentable over Olarig (US Patent No. 6,505,305)

As per claim 34, Olarig discloses:

A method of reading data from a self-testing RAM device comprising:

choosing a memory address (column 10 lines 59-67: data is read from a memory location, and the address is logged in the case of a fault);

retrieving data from a memory location associated with the address (column 10 lines 63-65: the data is read);

determining whether the data is correct (column 10 lines 59-67: logic determines if faults are present in the data);

correcting the data if it is incorrect (column 11 lines 3-20: if data is correctable, a failover process is performed); and

outputting the data to the requesting device, wherein the method disclosed hereby is performed by a self-testing RAM interface (column 12 lines 44-48).

The self-testing RAM interface further comprises a microprocessor, and the interface is part of a circuit board that includes the memory location (column 5 lines 13-17: a processor may execute the memory self-test, and column 5 lines 34-43: the memory is part of a central processing unit section, which includes a processor)

As per claim 35, Olarig discloses:

The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by utilizing an error correction code (column 5 lines 11-20).

As per claim 42, Olarig discloses:

An article of manufacturing comprising a computer usable medium having computer readable program code means thereon to perform the method of claim 34 (column 7 lines 43-46)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Callaway (United States Patent No. 6,879,530) in view of Lin (United States Patent 6,141,768)

Callaway does not disclose:

The system of claim 4, the self-testing RAM interface corrects errors by replacing erroneous data with redundant data stored in the memory array.

Lin discloses a testing system similar to Callaway's, in which defective memory cells are self-tested to determine if any defective memory cells are present (Lin figure 4

steps 154, 158). Lin takes the extra step of replacing the erroneous data with the correct data, skipping any memory cells that are determined to be defective (Lin figure 4 steps 162, 166). Callaway discloses that his system remaps failed memory bits to a different location when failures are detected (Callaway column 10 lines 55-59), but does not specifically state that the correct value is written to the remapped location. Callaway discloses that his invention is able to correct memory faults by remapping memory bits after they are operational, or "in the field" (Callaway column 2 lines 44-48). Writing the correct memory value to the remapped location would prevent any subsequent faults from occurring in the circuit, since the memory bit would be lost due to the failure of the memory location. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the remapping system of Lin into the remapping system of Callaway, preventing additional memory faults.

Claims 10, 24, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callaway (United States Patent No. 6,879,530) in view of Microsoft Computer Dictionary (fifth edition).

As per claim 10, Callaway does not disclose:

The system of claim 1, the memory array is associated with a field programmable gate array.

Callaway discloses that his system is designed to dynamically correct errors in a memory device (column 1 lines 6-11), and does not place any major restrictions on the memory array of his invention. An FPGA is a device designed to be updated and reprogrammed dynamically (Microsoft Computer Dicitonary definition: "FPGA"). Using Callaway's memory repair invention on an FPGA would enable the user to dynamically reprogram the FPGA and correct any memory faults that arise after the reprogramming. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate an FPGA into the memory repair system of Callaway, improving reliability after reprogramming.

As per claim 24, Callaway does not disclose:

The method of claim 22, the central processing unit is notified by generating an interrupt.

Microsoft Computer Dictionary defines an interrupt is a command which is sent to a processor, bringing its attention to a situation. The processor stops its other operations to deal with the cause of the interrupt. Callaway discloses that his system may include steps to repair a memory in a processor (column 1 lines 6-11). Using an interrupt would be a natural first step since it would stop the processor from attempting to complete other operations, and would not attempt to operate while its memory is still in a faulty state. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate interrupts into the testing system of Callaway, to prevent other processes from interfering with memory repair.

As per claim 28, Callaway discloses:

An article of manufacturing comprising a computer usable medium having computer readable instructions stored thereon to perform a method for testing a central processing unit (CPU) to memory interface comprising:

loading a data pattern [into CPU registers] (column 4 lines 48-58);

writing the pattern [from the registers] to at least a portion of memory in a memory device (figure 9 step 112)

reading the data written to each memory cell (figure 9 step 114);

comparing the data written with the data expected in accordance with the pattern (figure 9 step 116);

notifying the CPU if any data read is different than the data expected, wherein reading the data, comparing the data, and notifying the CPU are performed by a self-testing RAM interface (column 11 lines 18-25).

A second microprocessor embedded in a single circuit board with the memory device, the CPU and the memory device are formed of different integrated circuits (figure 6).

Callaway does not disclose:

Loading the data pattern into CPU registers

Writing the data pattern from the registers

Microsoft Computer Dicitonary discloses that a register is a high performance memory included in a processor which holds data for a particular process. Test pattern

generator 59 is part of test and repair circuitry 58 (figure 1), which functions as a processor, so it would be obvious to load the test pattern into registers before writing them to the memory blocks, as this is a well-known procedure in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate registers into the test pattern generator of Callaway, to store the test patterns before they are written to the memory blocks.

Claims 12, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callaway (United States Patent No. 6,879,530) in view of Wyatt (United States Patent 6,968,479)

As per claim 12, Callaway discloses:

The system of claim 1, the self-testing RAM interface comprises large geometry devices (column 4 line 63 – column 5 line 9)

Callaway does not disclose:

[the self-testing RAM interface comprises] ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory array.

Wyatt discloses an error memory verification system (column 4 lines 9-23) with ECC (column 6 lines 11-18). Wyatt discloses that ECC is a commonly used error correction method helpful in a wide variety of memory devices (column 2 lines 8-31). Callaway discloses that various patterns may be generated to be written to the memory blocks, including deterministic patterns (column 10 line 60 – column 11 line 17).

Additionally, Callaway discloses that the purpose of his invention is error correction. Using ECC would enable the Callaway's system to detect and isolate the errors in the memory effectively, without storing an entire mirrored copy. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC code into the memory testing system of Callaway, as a means for error correction.

As per claim 17, Callaway discloses:

The system of claim 14, the self-testing RAM interface comprises large geometry devices (column 4 line 63 – column 5 line 9)

Callaway does not disclose:

[the self-testing RAM interface comprises] ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory storage banks.

Wyatt discloses an error memory verification system (column 4 lines 9-23) with ECC (column 6 lines 11-18). Wyatt discloses that ECC is a commonly used error correction method helpful in a wide variety of memory devices (column 2 lines 8-31). Callaway discloses that various patterns may be generated to be written to the memory blocks, including deterministic patterns (column 10 line 60 – column 11 line 17). Additionally, Callaway discloses that the purpose of his invention is error correction. Using ECC would enable the Callaway's system to detect and isolate the errors in the memory effectively, without storing an entire mirrored copy. Therefore, it would have

been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC code into the memory testing system of Callaway, as a means for error correction.

As per claim 19, Callaway discloses:

The system of claim 18, wherein voting mechanisms determine the most probable data value to return from amongst the multiple copies (column 2 lines 64-67).

Callaway does not disclose:

error correction codes (ECCs) determine the most probable data value to return from amongst the multiple copies.

Wyatt discloses an error memory verification system (column 4 lines 9-23) with ECC (column 6 lines 11-18). Wyatt discloses that ECC is a commonly used error correction method helpful in a wide variety of memory devices (column 2 lines 8-31). Callaway discloses that various patterns may be generated to be written to the memory blocks, including deterministic patterns (column 10 line 60 – column 11 line 17). Additionally, Callaway discloses that the purpose of his invention is error correction. Using ECC would enable the Callaway's system to detect and isolate the errors in the memory effectively, without storing an entire mirrored copy. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC code into the memory testing system of Callaway, as a means for error correction.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouellette (US Patent No. 6,993,692) in view of Callaway (6,879,530), and in further view of Microsoft Computer Dicitonary (fifth edition).

Ouellette does not disclose:

The device of claim 20, voting mechanisms determine the most probable data value to return from amongst the plurality of stored copies.

Callaway discloses a voting system used to compare multiple sets of data in order to determine which data set is correct (column 10 lines 30-51). Ouellette discloses that a comparator may be used to compare the data sets, or the data values may be output for subsequent comparison by BIST circuitry. Callaway discloses that his system may be executed as a BIST system (column 2 lines 51-57). Therefore, Ouellette's system could output the results to the BIST system of Callaway to for comparison. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate testing system of Ouellette into the BIST system of Callaway, as a means to check for errors.

Ouellette and Callaway do not disclose:

error correction codes (ECCs) determine the most probable data value

Microsoft Computer Dicitonary defines Error correction coding as a method which detects errors in digital data by encoding it in such a way that it can be examined and errors can be detected and sometimes located. Callaway's system is also designed to detect and correct errors in a memory system (Callaway column 1 lines 6-11), as is

Ouellette's (Ouellette column 1 lines 10-16). Using ECC in the redundant system of system of Chen would enable the system to detect and correct errors on one of the multiple sets of data, or act as an additional failure indication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate ECC coding into the failover system of Olarig, as an added means of redundancy and reliability.

Claims 30-33, 36, 37, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (US Patent No. 6,505,305) in view of Hayes (US Patent 5,781,721).

As per claim 30, Olarig discloses:

A method for detecting hard errors comprising:

writing a test pattern to a plurality of memory cells in a memory device (column 10 lines 55-65);

reading the value of each memory cell containing a portion of the test pattern (column 10 lines 55-65);

recording the number times the value written did not correspond to the value read for each cell, wherein writing a test pattern, reading the value, comparing the value, and recording the number of times the value written did not correspond to the value read are performed by a self-testing RAM interface (column 10 line 65- column 11

line 20) and controlled at least by a microprocessor integrated with the self-testing RAM interface and the self-testing RAM interface with the microprocessor is embedded in the memory device (column 5 lines 13-17: the method may be executed by software on the host processor).

Olarig does not disclose:

comparing the value read with the value written to each cell;

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig discloses the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

As per claim 31, Olarig discloses:

The method of claim 30, further comprising:

determining whether any cell or cells have produced erroneous results more than a threshold number of times (column 11 lines 12-27);

determining whether any extra memory cells are available (column 11 lines 50-60); and

mapping any cells that have produced erroneous results more than a threshold number of times to available extra memory cells (column 11 lines 50-60).

As per claim 32, Olarig discloses:

The method of claim 31, further comprising notifying an exception handler if there are no available extra cells (column 11 lines 61-65).

As per claim 33, Olarig discloses:

The method of claim 30, wherein data regarding the number of times a cell value did not correspond to the value read is stored in a memory component located within the self-testing RAM interface (column 11 lines 10-25).

As per claim 36, Olarig fails to disclose:

The method of claim 35 wherein the self-testing RAM interface corrects incorrect data by retrieving a copy of the data from another data source.

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

As per claim 37, Olarig discloses:

The method of claim 36, wherein the data source is a magnetic disk drive (column 5 lines 43-45).

As per claim 39, Olarig discloses:

The method of claim 36, wherein the data source is one or more standard RAM devices.

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system

compares the read data with the data written to a memory, such as a cache RAM (column 1 lines 18-21), instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

As per claim 41, Olarig discloses:

The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by retrieving a copy of the data from another storage device and comparing the retrieved data and the copy.

Olarig's system uses an ECC system to detect faults in the memory device. Hayes discloses a similar memory testing system as Olarig, except that his system compares the read data with the data written, instead of using an ECC code (column 4 line 57 – column 5 line 5). This will make the correction capabilities of the system more accurate since each bit is compared to another bit instead of a parity type scheme as disclosed by Olarig. Olarig the limitations of ECC codes are such that not every error

can be corrected (column 2 lines 23-25), and that this causes the system to crash (column 11 lines 3-5). Comparing the data read to the written data would prevent such faults from happening, and prevent the system from being required to reboot frequently. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Hayes' testing system into the testing system of Olarig, increasing reliability and preventing crashes.

Claims 38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (US Patent No. 6,505,305) in view of Hayes (US Patent 5,781,721), as applied above, and in further view of Microsoft Computer Dicitonary (fifth edition).

As per claim 38, Olarig discloses:

The method of claim 36, wherein the data source is cache memory .

Olarig does not disclose any major restraints on the memory array 304 being examined in his system. It is only disclosed that the memory should be stored in blocks of 16, 32, etc. bytes, and have access to a memory bus (column 7 lines 37-42). A cache memory is a frequently used memory device which can access data quickly, and would be perfectly capable of meeting Olarig's restraints. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate cache into the memory testing system of Olarig, as a capable memory medium for testing.

As per claim 40, Olarig discloses:

The method of claim 39, wherein the RAM devices contain internal flaws such that the device is not fit for ordinary use (column 1 lines 8-12: the purpose of the system is to determine if there are flaws).

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 states:

The system of claim 1, the self-testing R.AM interface cooperates with a CPU to facilitate testing memory array data cells by dividing the memory array, so that each of the CPU and the microprocessor can simultaneously test the array thus facilitating faster testing of the memory array.

Response to Arguments

Applicant's arguments with respect to claims 11, 12, 14-23, 25-29, 34, 35, and 42 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 30-33, 36, 37, and 41 have been considered but are not persuasive.

Claim 34 is amended to contain the limitation:

The self-testing RAM interface further comprises a microprocessor, and the interface is part of a circuit board that includes the memory location.

Olarig discloses that a processor may perform the method of claim 34 (column 5 lines 13-17), and that the memory is part of a central processing unit station, which includes a processor (column 5 lines 34-43).

Claim 30 is amended to contain the limitation:

[the method is] controlled at least by a microprocessor integrated with the self-testing RAM interface and the self-testing RAM interface with the microprocessor is embedded in the memory device

Olarig discloses that a processor may perform the method of claim 34 (column 5 lines 13-17), and that the memory is part of a central processing unit station, which includes a processor (column 5 lines 34-43).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MTR

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